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Design and Analysis of Novel Cascaded Topology with LD Cell for Micro-source Grids

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Abstract: This paper focus on DC-DC converter called Novel Cascaded topology. This converter lies in the category of Non-Isolated DC-DC boost converters with upgraded voltage gain based on conventional topology with LD cell for micro-source grids. The proposed novel cascaded topology increases the voltage boost ability. There are some merits of our proposed topology that includes small voltages stresses across the switch, as well as upgraded gain. We prefered to use switch having small voltage rating as well as small resistance in ON-mode (R_{DS-ON}), it leads to provide high efficiency. In our cascaded topology with LD cell,we did not use large duty cycle, coupling inductors as well as transformer.We will utilize the Continuous Conduction Mode (CCM) for the analysis of proposed novel cascaded topology. This topology is designed to operated on 12V supplying voltage, 55% duty cycle, 265W output power and frequency of 12KHz. The continous conduction mode (CCM) has been analyzed theoretically as well as practically based derived equations. The novel cascaded converter has been simulated in PSIM as well as MATLAB/SIMULINK, while explanations of the overall results are provided based on PSIM.

Keywords: Novel; Cascaded; Topology; Micro-source; Application.

1. Introduction

Recently demand of power and consideration for renewable energy is increasing very fast because of different pollutions like global warming, environmental as well climate change by using fossil fuels. This makes the attention of researchers for making such generation systems that can utilize renewable energy sources to generate power. Distributed Generation (DG) systems are preferred for many renewable energy sources because it can provide various options to electricity consumers. The advantage of DG systems is that consumers get power direct from any source of them. Such systems not only meet the demands of consumers but can also act as power producer as micro-grid [1]. Micro-Grid is a new concept that defines the operation of distributed generation system. It takes up combination of many loads and micro-sources that is operated as an independent and on a single control system to provide power and heat to its restricted area [2]. Micro-sources are classified as high-frequency AC source and DC source. Both types contain multifarious applications of renewable energy, like fuel cells, piston-engines, modules of solar cells and turbines especially wind turbines [3]. Many micro-sources collectively provide voltage to a single micro-grid can be seen below in Figure 1 [4]. Renewable Energy (RE), which is created through micro-sources like fuel cells and solar cells have very low output voltage, it requires multiplier or series cells to upgrade the voltage to a proper level [5]

The use of series or multiplier cells makes issues like reduction in conversion efficiency, modules mismatching as well as partial shading. Similarly, there are more issues related to multiplies cells as conduction loss in components especially switches and inductors. It has been shown that we must operate the high power DC-DC boost converters through Continuous Conduction Mode (CCM). Current is disturbed due to little mismatch between two parallel modules [6].

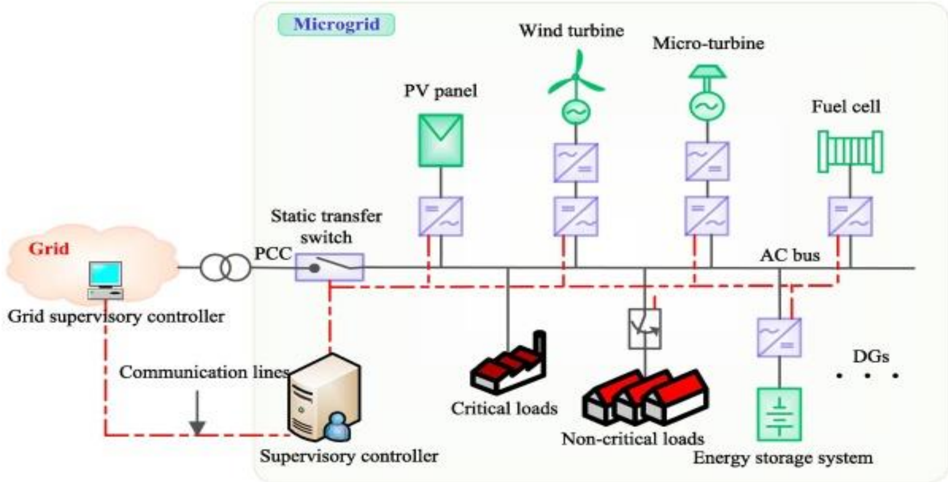

Figure 1. Schematic of the micro-grid consisting multifarious micro-sources and power converters [4]

The best solution to overcome the issue associated to micro-sources is to utilize DC-DC boost converter having high gain to upgrade the final voltage of micro-sources from low voltages to 380–400 V [7]. To convert high DC voltage in to AC voltages for AC appliances, DC-AC inverters are used [8]. All micro-sources produce low DC voltages which are not suitable for different applications, so there is significant need of dc-dc boost converters having high gain to increase the level of voltage based on required applications.

2. Literature Review

There are many research papers that have been published for micro-sources including conventional or traditional boost converter, which has limited static gain in practice [9]. Traditional boost converter topology is not suitable to utilize in higher-power application because of considerable switching loss [10]. Similarly, on-state resistance and sometimes unity duty cycle cause large conduction loss due to voltage gain is reduced [11]. Another common issue is the equivalent series resistance (ESR) of components also plays role in the reduction of voltage gain [12]. Parallel combination of many boost converter gives the concept of interleave topology also utilized to upgrade the voltage gain, performance as well as to overcome the size of inductors [13]. Due to many number of phases, the switching frequency becomes large and current passes through different branches. In spite of these, the size of the electromagnetic interference (EMI) filter and energy storage inductors are able to be overcome. [14]. Beside these improvements of some performances, there are some disadvantages including increasing weight, high costs, voltage spikes, as well as leakage inductance [15]. To reduce such problems, half-bridge flyback converters, switched capacitors and snubber circuits are proposed in [16].

Different techniques are used to upgrade voltage gain of DC-DC boost converters by utilizing diodes, inductors and capacitors as proposed in [17]. Reduced ripples in current as well as upgraded gain of voltage are possible; many traditional boost converters are utilized in series connection or cascaded. To maximize the reduced voltage that is given at input, high duty cycle value is used in first phase. The second phase of cascaded topology decreases the power loss in switches while utilizing small value of duty cycle. In this case, the designation of controlling part is important. Similarly due to large number of components, the robustness is compromised [18].

Some new approaches have been used in cuk converter topologies [19] for increasing their voltage gain, yet it has low efficiency and using large number of switches, inductors and other components, which are the major cons.

To increase the voltage gain, coupled inductors have been applied in various DC-DC boost converters [20]. Leakage inductance is used to restrain falling rate of current in diode, which limits the reverse-recovery issue of diode. Moreover, transformers can be replaced by coupled inductors to decrease the duty cycle as well as extra fluxes in DC-DC boost converter [21]. The hindrance of DC to DC attractively coupled inductor support converter is the leakage inductance issue. In order to overcome the leakage issue, active as well as passive circuits have been used with coupled Inductor Topology [22]. In case of Switched Inductor Topology, the voltage gain is linked with the duty cycle. By changing duty cycle, it varies the voltage gain. Similarly, this topology needs small number of levels for gaining greater value of gain and efficiency with lack of using very high duty cycle, but it has low input and output power [23]. It is required to have maximum gain in between 50-60% duty cycle, reduced voltage stresses, high efficiency, minimum modes of operations as well as low number of components.

This paper presents a Novel Cascaded Topology with LD Cell for increasing the final voltage of a micros-source to a level of voltage that is required by specific application. This new circuit lies under quadratic topology, it composed of conventional and inductor-diode cell. The configuration of our proposed topology is given in Figure 2. This topology is formed of two converters namely conventional or traditional & switched inductor.

For the explanation, the proposed topology is divided into two stages called first stage and second stage. The first boost stage acts as step-up converter, which contains one Input-Inductor L1, 2 Input-Diodes as D1 & D2, as well as Input-Capacitor C1 for pumping. Second stage is LD cell, which contains two-Inductors as L2 and L3, three diodes D3, D4 and D5, and one output capacitors Co. While both stages are operated with single switch S using gate G1 signal.

The single switch of proposed topology is controlled by gate signal as a result minimization in the control strategy is achieved. As the voltage gain of both stages depends upon one duty cycle, output voltage is controlled within the required range.

This paper consists of many sections. Introduction is presented in section 1, literature review is presented in 2, and operating principles are given in 3, equations are analyzed in 4, simulations results are explained in 5 and overall research paper is concluded in section 6.

3. Operating Principles of the Proposed Converter

Our proposed new D-DC boost converter i.e. cascaded topology is utilized to increase the different voltage levels based in unique multiple number. The configuration of new cascaded topology contains two parts namely traditional or conventional and LD Cell, while LD cell is composed of inductor and diode. There are many advantages of new cascaded topology over conventional ones. It has upgraded voltage gain, high efficiency, reduced voltage ripples, small voltages stresses across the switch as well as better transient response. The whole configuration of cascaded topology can be seen in Figure 2.

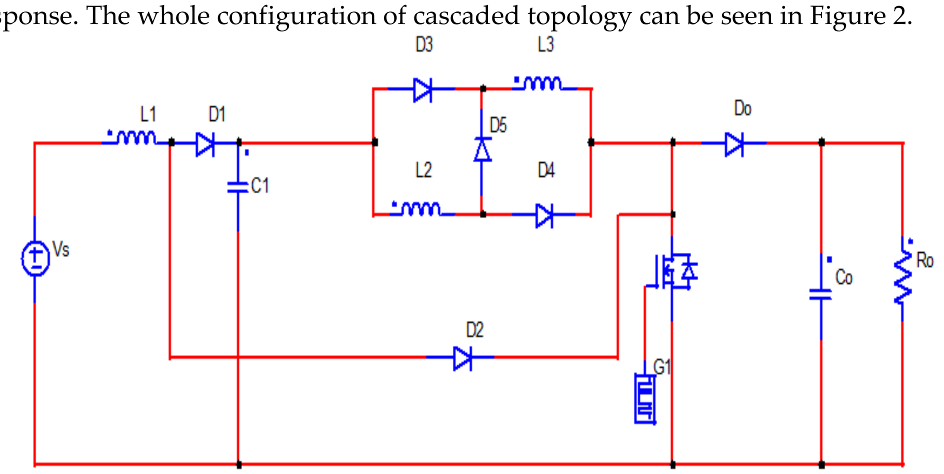

Figure 2. Proposed Cascaded Topology

In our proposed new cascaded topology, whole conversion of voltage depends on switch that switches form input part to output periodically. The configuration of new topology contains six-diodes, three-inductors, two-capacitors. The operating principle is nearly same as the operation in quadratic topology. There is only small difference that is due to LD-cell. The proposed topology used only one switch for its switching. In our new cascaded topology, the LD-cell is used in place of inductor as in quadratic topology.

The operating principles of new cascaded topology consists of two modes of operation, namely ON mode and OFF mode.

3.1. ON Mode

In this mode of operation, the switch is brought to conduction mode by turning on it. In the beginning, inductor L1 gets charge nearly equal to the voltage provided by source by using Switch and diode D2. The overall current passes through inductor L1, D1 and switch and then returns to voltage source. As when OFF mode ends, the capacitor C1 is discharged to L2 & L3. The inductor L2 is charged by D4 and inductor L3 is charged by D3 respectively. Most importantly, both inductors L2 & L3 have same voltage storages. Figure 3 shows the overall phenomenon of the proposed topology.

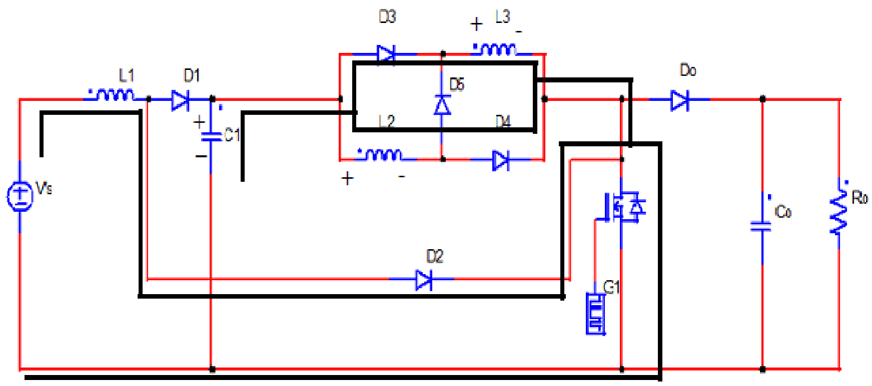

Figure 3. Conduction-Mode (ON Mode)

3.2. OFF Mode

In this mode of operation, the switch is brought to insulation mode by turning off it. The inductor L1 is discharged to capacitor C1 through D1 which is in forward biased. The diode D2 becomes reverse biased. During OFF mode, the inductors L1 & L2 change their polarities and act as in series to transfer power to output part of circuit especially capacitor Co as shown in Figure 4.

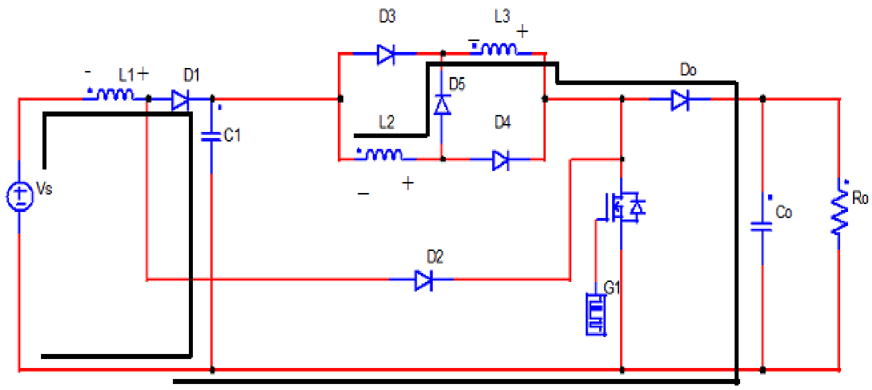

Figure 4. OFF-Mode

4. Steady State Analysis of New Cascaded Topology with LD Cell

The analysis of the proposed topology is performed based on it steady state operation. The steady state waveform is shown in Figure 5. The overall suppositions are considered as ideal with efficiency of 100%, Input-Voltage V_s is pure DC as well as capacitors are sized having nearly small voltage-ripples at given Switching-Frequency (f_s).

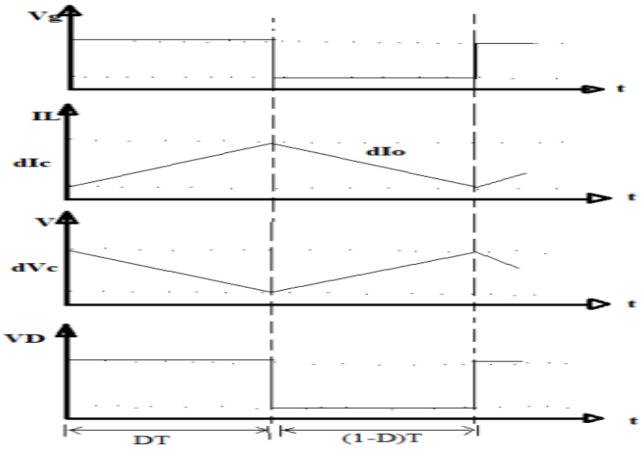

Figure 5. Steady State Waveform

We already showed that the proposed circuit consists of two portions namely traditional and Switched-Inductor (LD)-cell. Primarily, we will analyze the first part with its both modes.

When the switch is turned on like in Figure 3, inductor L1 stores power that can be derived as in equation (1);

$$V_{L_1}(t) = V_S \quad (1)$$

Equations (1) can be rewritten as:

$$V_S = V_{L_1}(t) = (L_1).\frac{dI_L}{dt} \quad (2)$$

Where $\frac{dI_{L_1}}{dt} = \frac{dI_L}{dt}$,

Then,

$$\Delta I_C = D.\frac{V_{L_1}(t)}{L_1} \quad (3)$$

Using Equation (1) in Equation (3), we get

$$\Delta I_C = D.\frac{V_S}{L1} \quad (4)$$

When the switch is brought to off mode as shown in Figure 4, we apply Koirchoff's Voltage Law (KVL) to find the equation of voltage across inductor V_{L1}:

$$V_S = V_{L1}(t) + V_{C1} \quad (5)$$

In equation (5), V_{C1} shows the capacitor C1 voltage.

$$V_{L1}(t) = V_S - V_{C1} \quad (6)$$

When the Switch is turned off, then the VL1 Second-balance can be written as:

$$\Delta I_O = (1-D).\frac{V_{L_1}(t)}{L1} \quad (7)$$

Putting Equation (6) in the above equation (7),

$$\Delta I_O = (1 - D).\frac{V_S - V_{C_1}}{L1} \quad (8)$$

For finding the average current, the current thorugh L1 in off mode is added to current through L1 in on mode and then make them equal to zero.

$$\Delta I_C + \Delta I_O = 0 \quad (9)$$

Use the equaitons of current in both modes in equation (9);

$$D.\frac{V_S}{L_1} + (1 - D).\frac{V_S - V_{C_1}}{L_1} = 0 \quad (10)$$

$$DV_S + (1 - D)(V_S - V_{C1}) = 0 \quad (11)$$

$$V_S - V_{C1} + DV_{C1} = 0 \quad (12)$$

$$\frac{V_{C_1}}{V_S} = \frac{1}{1-D} \quad (13)$$

For finding the overall gain, $\frac{V_O}{V_S}$ =?

Apply Voltage-Inductor-Second Balance quation on Inductior L2 as well as L3 in both modes of operation. As both inductors have same values of inductance.
During OFF mode, the Voltage-Second Balance equation can be expressed as:

$$\Delta I_C = \frac{V_{C_1}}{L} D \quad (14)$$

During ON mode, the Voltage-Second Balance equation can be expressed as

$$\Delta I_O = \frac{V_{C_1} - V_O}{2L}(1 - D) \quad (15)$$

When both equations of Voltage-Second Balance are added gives average current through both inductors:

$$\Delta I_C + \Delta I_O = 0$$

Use the equaitons of current in both modes in equation (9):

$$\frac{V_{C_1}}{L} D + \frac{V_{C_1} - V_O}{2L}(1 - D) = 0 \quad (16)$$

$$V_{C1} D + V_{C1} - V_O + V_O D = 0 \quad (17)$$

$$V_O = \frac{(1+D)}{(1-D)} V_{C1} \quad (18)$$

Use equation (13) in equation (18);

$$\frac{V_O}{V_S} = \frac{1+D}{(1-D)^2} \quad (19)$$

$$V_O = \frac{(1+D)}{(1-D)^2} V_S \quad (20)$$

The equation (20) shows the gain of the proposed topology that is nearly about 6 times of voltage that is given at input with 55% duty cycle.

We have been compared four different topologies at different values of duty cycle. We concluded that there is no considerable difference in voltage gain of all topologies when they are operated on low duty cycles. For values of duty cycle higher than 50%, we noted the considerable difference among all topologies, as the voltage of novel cascaded topology is higher than other three topologies as shown in Figure 6. So, we concluded that proposed topology must be operated in between 50% and 90% Duty Cycle for gaining upgraded gain.

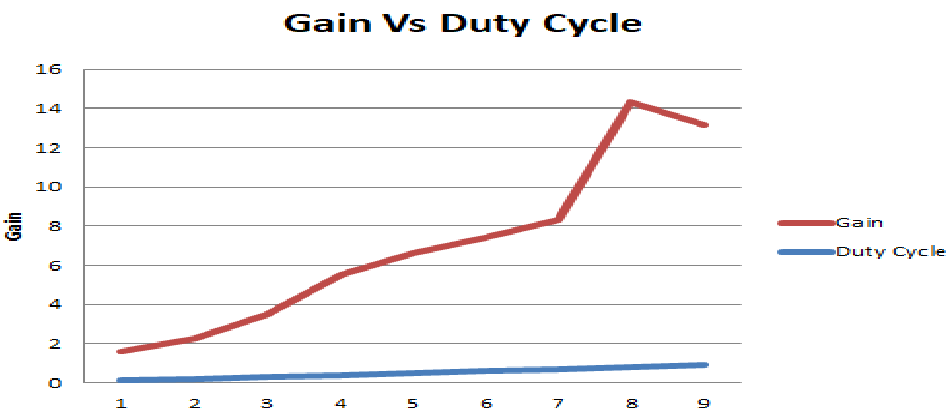

Figure 6. Gain Vs Duty Cycle

5. Simulation Results

To verify the theoretical concept and analysis of our proposed novel cascaded converter with LD-cell. We evaluate the proposed topology in Continuous Conduction Mode (CCM). The circuit was simulated on PSIM Software with its detail simulation results. The new cascaded boost converter with LD cell has been simulated on the parameters given in Table 1. The parameters are selected based on the gate signal frequency of 5 kHz, 12V as Input-Voltage, 55% duty cycle and then we achieved 73.9V as the final output voltage.

Table 1. All Parameters with their values

Parameters	Values
Input Voltage	12 V
Inductors L1=L2=L3	300 uH
Capacitors C1	30 uF
Output Capacitor Co	40 uF
Output Resistor Ro	15 Ohm
Duty Cycle D	50%
Output Power Pout	215.51 watt
Switching Frequency	5 KHz
Input Power Pin	243.51 watt
output voltage Vo	73.9 V

During ON-mode, the inductor L1 acts in series with source as well as D2, the source current (Is) at that moment is maximum, while during OFF mode, the source current becomes half of its maximum values as shown in Figure 7.

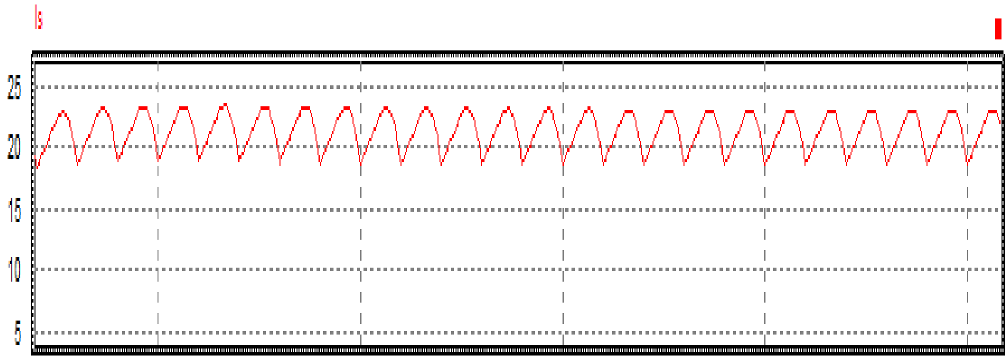

Figure 7. Souce Current (Is)

For getting output parameters, the output is taken from output resistor. To get maximum output voltage, the output current was already reduced by changing components. When the output current is 3.66A then we achieved 73.9V as the output voltage as shown in Figure 8.

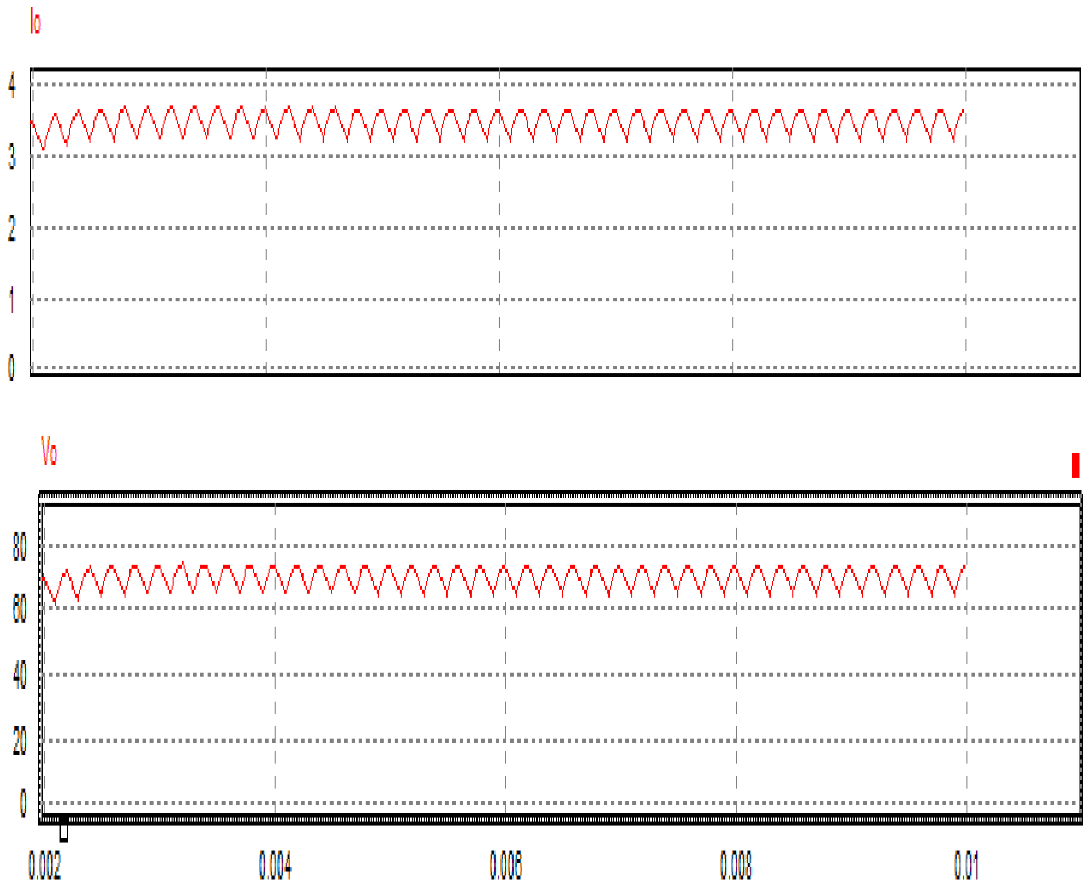

Figure 8. (a) Output-Current (Io), (b) Output-Voltage (Vo)

The proposed topology has reduced voltage-stress compare to conventional and switched inductor topologies across the switch that can be seen in below Figure 9.

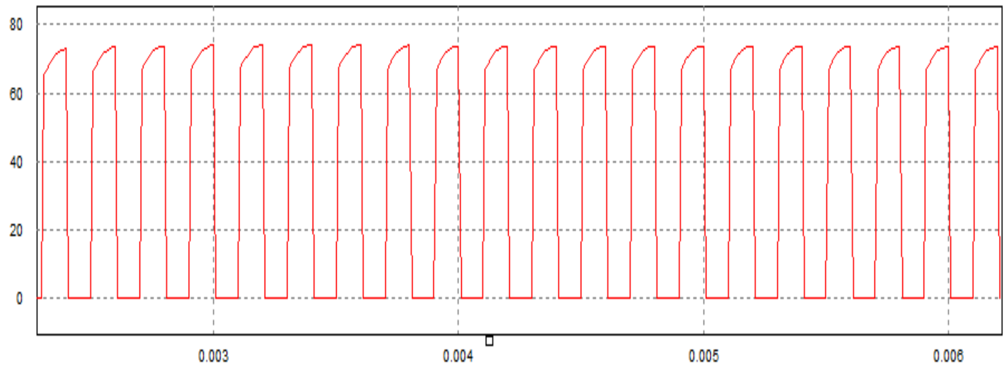

Figure 9. Voltage Stress on Switch

The output voltage of boost converter usually depends upon the values of duty cycle. The duty cycle is figured out based on PWM signal. The whole cycle is divided into two parts that is ON and OFF. For high duty cycle, the large part is given to ON mode and vice versa. In this case, we have given 55% duty cycle due to which 55% part of whole cycle is covered by ON mode as shown in Figure 10.

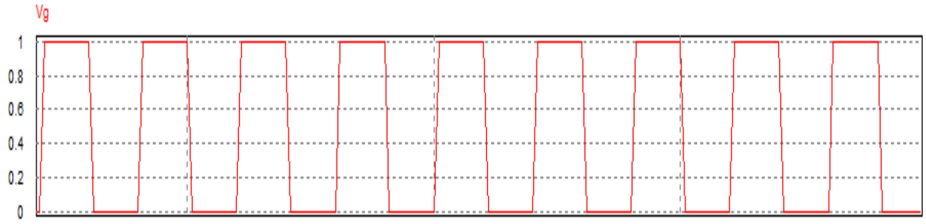

Figure 10. PWM-Signal

Different diodes show different voltage stresses. The voltage stresses across D1, D2 & D5 are nearly identical. In case of D3 & D4, the voltage stresses are identical as shown in Figure 11.

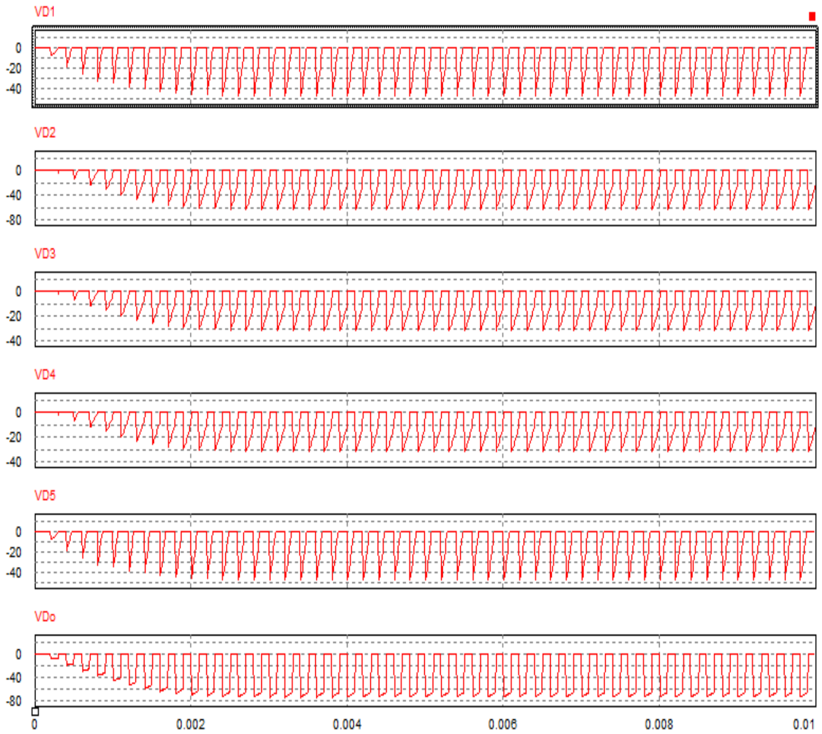

Figure 11. Voltage Stress across each Diode

There are only two capacitors, which are used in circuit that are C1 and Co. The voltages across both capacitors are shown in Figure 12. The capacitor Co is used to filter out the output voltage, as Vco is nearly identical to output voltage.

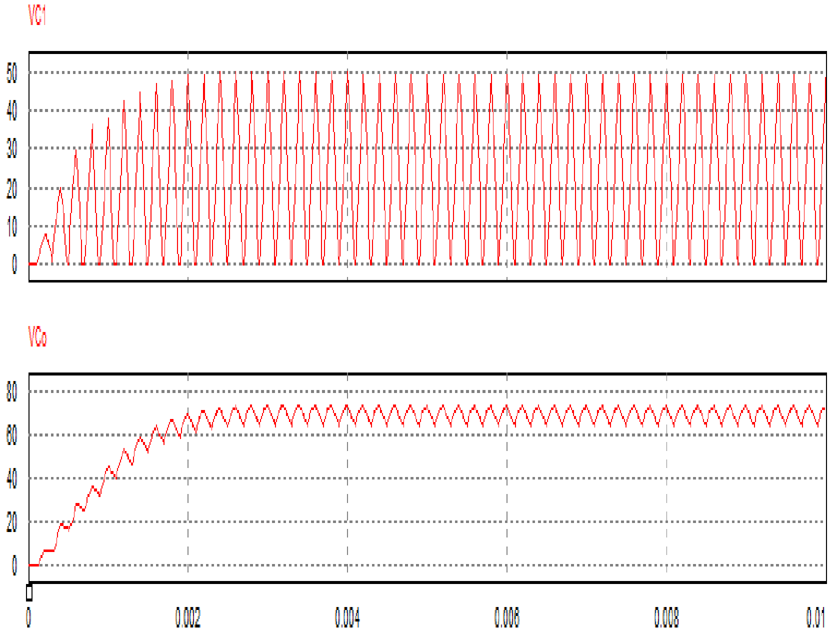

Figure 12. Voltages across C1 and Co

There are three inductors, which are used in proposed topology. The voltage across L1 is different than other two inductors L2 & L3, which are same in inductance as well as voltage values as shown in Figure 13.

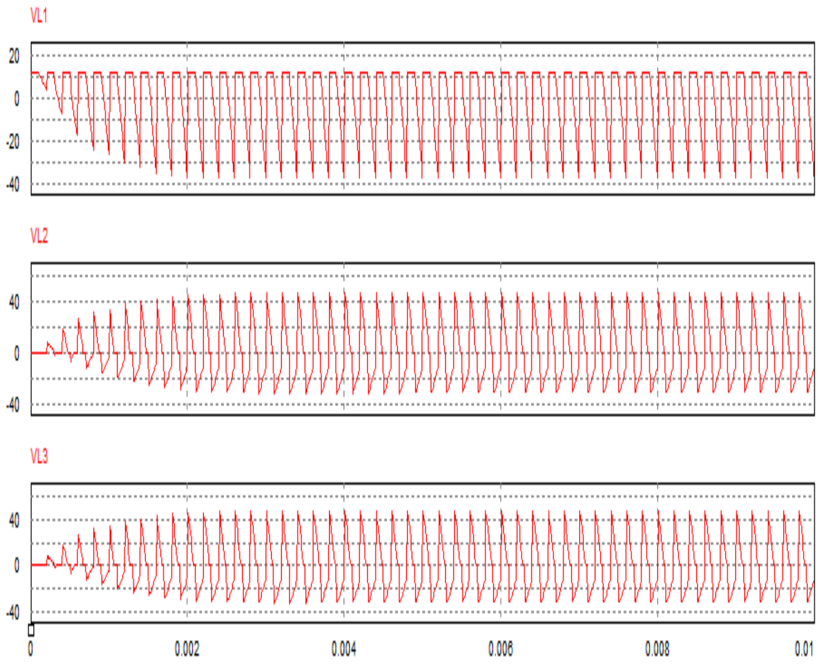

Figure 13. Voltage across L1, L2 & L3

The source current as well as current through L1 are same but different than current through L2 and L3 which are same in inductance and current values as shown in Figure 14.

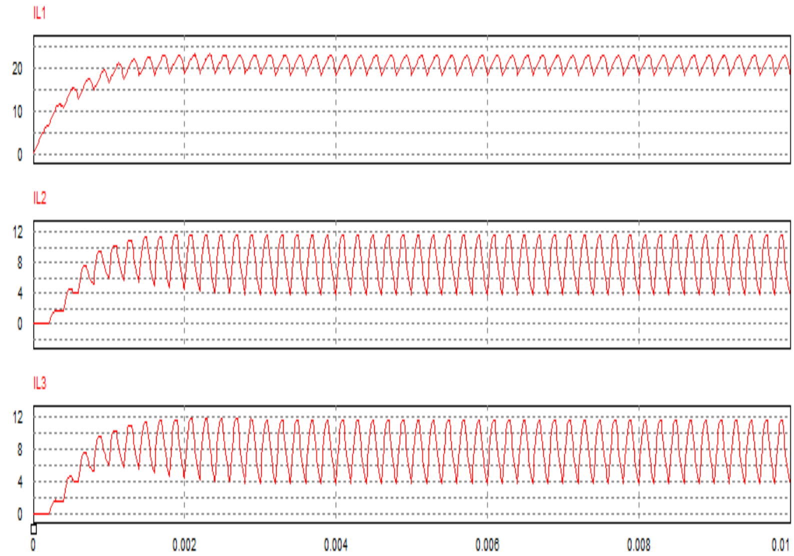

Figure 14. Current through L1, L2 & L3

We analyze the novel cascaded topology for getting high efficiency based on different values of duty cycle. The efficiency shows decreasing between 0.1 and 0.3, while it shows increasing between 0.3 and 0.55, when we increase the duty cycle further, it again decreases the efficiency. So we specified the value of duty cycle at 0.55 at which the new cascaded topology shows maximum efficiency.

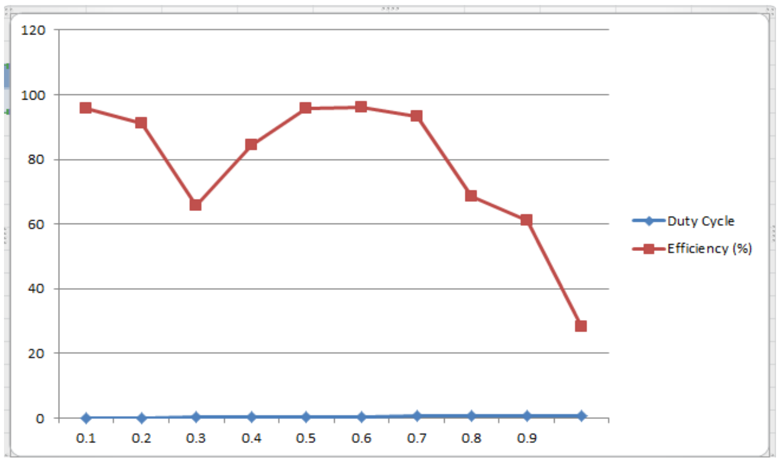

Figure 15. Comparison: Efficiency Vs Duty Cycle

6. Conclusion

This article proposes a new DC-DC boost converter termed as novel cascaded topology with LD-cell. This study has brought a new proposed topology with low switching loss as well as high voltage gain. It has been designed without using the coupled inductor or transformers as well as not operated on high duty cycles. The proposed new topology is able to produce output that is approximately six-times of voltage that is given at input. The circuit is analyzed in Continuous Conduction Mode (CCM). If the input voltage is 12V then the output voltage will be 74V. Novel cascaded topology has been simulated by using PWM technique having uniform frequency. The proposed topology has many advantages including upgraded voltage gain, small switching loss, high efficiency, low complexity, low cost and simple design of circuit. Both stages of the proposed circuit are completely analyzed to get final equation for voltage gain. All simulation results confirm the mathematical equations and modes of operations.

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