

# Integrated Power Combining and Amplification for Compact S-Band Radar Transmitters

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Received: February 01, 2025 Accepted: March 31, 2025

**Abstract:** This paper deals with one of the major problems in high power S band radar transmitters by discussing the design, simulation, fabrication, and validation of a compact, high performance Wilkinson type power divider with amplifier impedance matching network. Till now, traditional Wilkinson Power Dividers (WPDs) tend to focus on isolation and return loss but are poor in amplitude balance throughout the wide frequency ranges especially in high power and space limited applications. The architecture proposed is applicable for a 1 kW S-band radar transmitter and focuses on minimal amplitude imbalance ( $\leq 0.75$  dB), compact, return loss better than  $-12$  dB. When simulations were conducted using Advanced Design System (ADS) software, performance was shown to be strong with insertion loss between  $-12.18$  dB and  $-12.50$  dB, return loss more than  $-18.65$  dB, and isolation more than  $-25$  dB in the bandwidth, 2.7–3.0 GHz. The design was built using a Rogers RT/Duroid 5870 substrate, the design utilized a 75W PH2731-75L RF transistor with optimized impedance matching to have a high power dissipation. Simulations came relatively close to measurement results, which confirmed the effectiveness of the design. This work helps to build compact and efficient RF front end modules for radar that can be upgraded from the insertion loss and future applications wise.

**Keywords:** S-Band Radar Transmitter; Wilkinson Power Divider; High-Power RF Design; Power Amplifier Integration; Impedance Matching.

## 1. Introduction

S-band modern radar transmitters require strong and effective power delivery mechanisms in order to provide the needed generation of high-power and well-direction electromagnetic signals [1]. The heart of this functionality; power divider, is a basic RF component that splits the input power evenly across multiple amplifier stages. Such proportionality is critical to proper coherent amplification and maximum power output of the transmitter as a whole. In the plethora of Power Divider topologies, the Wilkinson Power Divider (WPD) is being currently customized to be the most preferred choice for High Frequency applications with superiority of capabilities of equal power split, excellent isolation between the output ports, and optimal impedance matching all of which contribute to amplifier performance and reduce signal reflection/loss [2-3].

In high-power radar systems with parallel amplifier configuration, the need of multiple mode power divider, usually 8-way or 16-way has grown more acute [4]. Nevertheless, as it turns out, an increase in the number of output ports results in a dramatically complex design and practicality of Wilkinson dividers. High-port-count WPDs have a number of issues such as; circuit layout complexity, reduced PCBs space, insertion loss, degradation of isolation and limit on bandwidth. Furthermore, both fabrication constraints and cost implications grow increasingly critical as the designs increase in size and complexity. Thereupon,

balancing electrical performance and physical reliability plays a critical role in development of such systems. In designing these distribution networks, the primary design parameters such as insertion loss, return loss, isolation and impedance must all be carefully optimized to ensure the network maintains its effectiveness and reliability [5].

This research discusses these challenges by providing the design, simulation, fabrication, and experimental validation of a high performance Wilkinson power divider that is specifically tailored for a low to medium altitude radar transmitter. The proposed design is designed to outperform the constraints presented by the high-port-count configurations providing the least amplitude imbalance, excellent isolation, and well-matched impedance through a wide band of frequency. By incorporating this power divider with optimal power divider in amplifier matching network combination, the system presents efficient power transfer and improved operational performance. This design's successful implementation will advance the production of next generation radar systems with better power efficiency, longer range, and overall system effectiveness [6-7].

### 1.1. Research Objectives

The scope of this research concerns the design, simulation, and real implementation of a high-efficiency Final Power Amplifier (FPA) to be applied for 1 kW S-band radar transmitter. The drive to satisfy rigorous performance benchmarks and physical constraints common of modern radar system has powered the research. The main targets of this work are listed as below.

**Power Delivery:** To design an amplifier system capable of reliably delivering an output power of 1 kW.

**Frequency Coverage:** In order to guarantee both steady and efficient operation throughout the delineated S-band frequency band, 2.7 GHz to 3.0 GHz.

**Power Division Strategy:** To find configuration for dividing input power into several equal paths and to specify the final structure of this structure based on a trade off between electrical performance and practical implementation parameters.

**Amplitude Consistency:** For maintaining amplitude variation of 0.75 dB over all output ports to allow for a uniform signal distribution.

**Impedance Performance:** To obtain return loss values better than -12 dB at critical interfaces, such as the power divider input/output and the impedance matching networks of the RF power transistor; which hence reduces signal reflection.

**Space Optimization:** To design the system in a compact footprint consistent with the limited space usually available to S band radar hardware environments.

These objectives will enable the project to handover a reliable and compact high power amplifier solution for integration with advanced radar platforms.

## 2. Literature Review

Important technological advancements in radar and communication systems have exposed a high need for very efficient power dividers, combiners, and amplifiers. Among the major drivers behind this demand is the continued trend towards solid state devices like Gallium Arsenide (GaAs) and Gallium Nitride (GaN) that have been able to dramatically improve the amplifier efficiency, thermal control, and size pressure in today's transmitters [8]. These improvements have made it possible to build smaller and more powerful radar systems that can work on a higher frequency and better performance. However, however modern the world is now when it comes to solid state technology, there is still the need to maintain and upgrade the existing radar systems to particularly legacy solid state transmitters which is imperative. There is a high number of currently fielded radar systems that need sustained lifecycle support and the solid-state transmitter design is still of fundamental importance to the operational longevity of a radar system. Such transmitters are optimized in regards to such key performance parameters as amplitude imbalance, isolation, and return loss (VSWR) for improved stability and the detection of the target, with specificity over the operating frequency band [9].

In view of the radar system, the Final Power Amplifier (FPA) is a very important component of the transmitter that provides high power to the transmitter's antenna for the reason that a strong signal will

be amplified in order for it to be detectable over a greater distance. This research is more concentrated on the design and development of a high power FPA for an S-band radar system with the objective of attaining optimal levels of performance relative to the operating frequency range, insertion and return loss, isolation, and amplitude imbalance. Such parameters are essential to functioning of the radars since they impact the signal integrity and efficiency of power usage, as well as general reliability. The main goal is to achieve the lowest insertion loss and highest gain linearity, and not to have any large amplitude imbalance across the desired frequency band [10]. While chasing performance goals are not easy especially for high-power systems when heat dissipation, power distribution and impedance matching demand are paramount.

The review of the existing literature on power divider/combiner architectures shows that there is quite a lot of diverse designs to which power dividers/combiners are employed in radar and communication applications such as Wilkinson power dividers (WPD), T-junctions, ring couplers and hybrid junctions. Each of these architectures has their own set of benefits and trade offs that determine their applicability with particular application. Among them, WPDs (W accumulation versus P accumulations) have become widely adopted in radar systems because of their outstanding performance features. Wilkinson power dividers can split or combine power signals without damaging the characteristics of the signals. They are created to deliver matched terminations on all ports so that they will work losslessly when all ports are properly matched. Additionally, WPDs provide exceptional isolation between output ports and thus strongly minimize signal leakage, which is easier to implement than other types of dividers or combiners [10-11]. Such benefits develop because of the application of wave transformers where impedance of the split ports are equated to the common port, hence easy passing of power. These properties have made WPDs an ideal choice in radar applications where performance must be high, signal distortion low.

A review of the relevant literature identifies many important contributions towards the evolution of WPDs, in particular from the perspective of radar systems. Mohra (2008) suggested a compact design of dual-band WPD using a quarterwavelength transformation section to ensure size reduction without degrading performance [12]. Although convenient for miniaturization purposes, the current design has to be substantially modified for high power (1 kW) operation in S-frequency band and reliable operation must be assured. Mahardika et al. (2016) proposed a modified 1:4 WPD configuration for use in the S-band, which allowed for insertion loss of below  $-8$  dB on each of the output ports and this provided the feasibility of power division in the desired frequency band [13]. Their research is informative in design of WPDs for the S-band specifically to high power handling applications.

Gysel (2012) met the challenge of high power operation of WPDs by suggesting an N-way design with high power resistive loads [14]. This design, aimed at the 1.02–1.25 GHz range, shows compelling performance in VSWR, insertion loss and power handling. Although the design targets a different frequency band, the design provides some critical insight into design considerations for the high-power-application. On the other hand, Kumar and Prakash (2019) investigated different multi-port WPD arrangements (2:1, 4:1, 8:1, and 16:1) for L-band applications (1.0–2.0 GHz), which offer useful lessons with regard to the trade-offs between the number of output ports, design complexity, and overall performance [15]. Their work is oriented in another frequency range, yet the knowledge they acquired during their estimation of multi-port WPDs supported our choice of the number of S-band WPD for outputs, taking into account the trade-off between the amplitude linearity, completeness of shape, and the requirement for the compact design within the antenna and the limitations of space in the radar system.

Santiko and Darwis (2016) presented a WPD that was two-band in nature for use in radar applications that use the meander line approach that reduced the size of the device without compromising power division efficiency [16]. Their work draws attention to the need to achieve excellent isolation in between output ports so that there is minimal signal leakage, which is on crucial consideration for optimal performance of WPD. The use of the meander lines also makes the design compact and efficient, and it is highly relevant in the case of a radar system where space might be constrained.

Although the literature supports the use of WPDs for S-band radar transmitter applications [17-18], a major gap still remains in terms of development of S-band WPDs optimized for high-power operation. Previous research studies have mainly reported good work on achieving good insertion loss, isolation, and return loss while ignoring the need in gain flatness through the entire frequency band and minimum amplitude imbalance for high-power ( $>1$  kW) radar amplifiers. Fundamental criteria for effective operation of a power divider/combiner in high-power radar systems, these have not been the main focus of existing

research. This research is aimed at resolving this gap with the design of a compact, high performance, divide/combine which maintains minimal amplitude imbalance, best isolation matching while working effectively at power levels of 1 kW and above.

Addressing these critical design considerations, this research will advance high power radar systems, providing more efficient, and reliable and cheaper modern radar and communication applications.

### 3. Material and Methods

The research commenced with designing of proposed WPD in Advanced Design system (ADS) 2016. After successful simulations, transistor impedance matching was implemented using smith chart utility tool available in ADS-2016. With the help of simulation results, it was proved that the WPD design of 1:16 power divider/ combiner achieves insertion loss of -12dB with amplitude variation better than 0.75dB. After fabrication, scattering parameters of proposed design were measured with the help of Agilent vector network analyser part number E5071C [19].

#### 3.1. System overview

The goal of this research is to create a high-power amplification system targetting high-powered boosting from 250 W input signal to over 1 kW using a parallel arrangement of 16 RF transistors. This approach uses the output of a number of transistors together to achieve the required power gain efficiently over the full 2.7 to 3.0 GHz range of frequencies involved. There is a 250 W input from a pre-amplifier that is input to the 16 RF transistors equally. Each transistor draws around 15.6 W of power guaranteeing that all transistors operate within their power handling limits and thus minimizing the dangers of overloading any individual device.

To achieve this application's constant and reliable power amplification within the specified frequency range, the PH2731-75L transistor was used because it can offer high output power of 75 W within the 2.7 – 3.0 GHz band. This transistor is also ideal for high power application, with optimum performance with minimum distortion, it is also specially designed for high efficiency operation in radar system. The strength of the PH2731-75L transistor makes it possible for it to keep output power consistent despite dealing with high-frequency signals and thus an appropriate option for this application [20-21].

After the input power is allocated to each one out of the 16 transistors, the amplified outputs are then combined using a large power 16 way power combiner. The combiner is additive enough to add individual outputs of transistors to produce final output power above 1 kW; the target for this research. The task of the power combiner is make the phase and amplitude of the combining signals from all the transistors to be appropriately aligned, thus maximum output power is achieved as well as ensuring zero destructive interference between the signals. This system can be divided into two main components viz design and operation:

- i. 16-Way Power Divider/Combiner: This part of the amp splits the incoming signal equally across 16 RF transistors and combines the outputs from all 16 transistors back into one high power output. The splitter / combiner must be designed very carefully to ensure that the power is equally distributed to each of the transistors in one direction while the second such structure will be used for a combined input from the transistors while ensuring that the right matching of impedance is observed in the process to prevent signal loss or reflections.
- ii. Transistor input and output impedance matching design. Impedance matching is fundamental to power transfer at maximum level and rejection of reflections in the system. Power that is transmitted to each transistor is efficiently transferred due to proper impedance matching, hence there is no power loss occasioned by mismatched impedances. Also the impedance of each transistor's output should be matched against the input impedance of the combiner to make sure that the overall output being combined is of maximum quality positive feedback.

The system design overall is orientated to obtain the best performance, with equal power supplied to each transistor and high efficiency in power amplification with a final output surpassing 1 kW with as little loss or distortion of the signal as possible. As seen in Figure 1, the system operation is illustrated through the power divider and transistors and the combiner which will produce the desired high-power output.

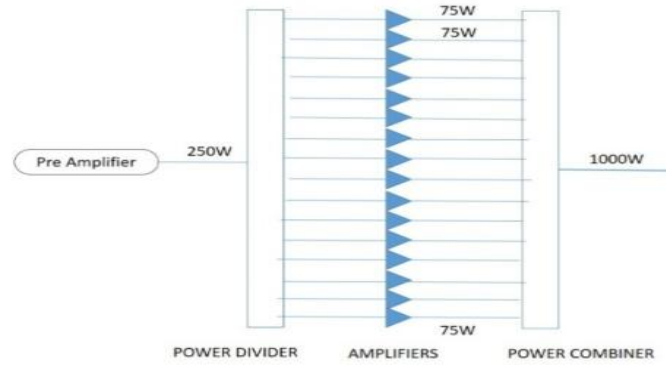


Figure 1. The Overall System Architecture

3.2. Design Strategy and Challenges

The design is applied with Rogers RT/Duroid 5870 substrate that was selected due to its excellent low-loss characteristics for high power operation as well as for its overall cost-effectiveness [22]. This substrate is ideal for high power amplification applications because it provides low dielectric loss and is dependable when supporting signal integrity under heavy powered conditions. Table 1 below summarizes the main specifications of Duroid 5870.

Table 1. Substrate Specifications

Material	Duroid 5870
Dielectric constant	2.33
Substrate Thickness	0.787 mm
Loss Tangent	0.0012
Copper Thickness	35um
Thermal Conductivity	0.22 W/K*m

Rogers’ microwave impedance calculation tool was invoked to find out the power handling capacity of the transmission lines. The amplifier is engineered to offer maximum output power of 1 kW at 10% duty cycle. This gives a mean power requirement of roughly around 100 W. As shown in Figure 2, microstrip transmission lines can support power in the order of average power levels of up to 500 W.

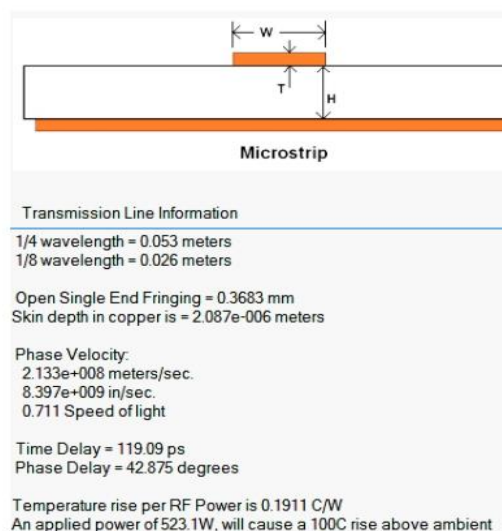


Figure 1. Transmission Line Power Handling Using Line Calc. Tool

Based on the maximum operating temperature of 100°C and ambient temperature of 25°C, the average power-handling capacity of the transmission line is further calibrated. With these parameters, it can be concluded that the microstrip transmission line can effectively support average power levels that do not

exceed 331 W without degrading performance and efficiently transferring power, thereby enjoying safe system operation during the actual operating condition.

### 3.3. Designing Advanced Design System (ADS)

With prevailing designs on a Wilkinson Power Divider (WPD) for our particular application being unknown, a phased design strategy was employed in order to achieve the established objectives. The process started with a 2-way WPD, then moved through higher-order configurations. The original design was applied to a Rogers 5870 substrate in the Advanced Design Systems (ADS) environment. The microstrip transmission lines were developed using the MLIN component of the ADS library to form layout of the 2-way divider/combiner. Impedance and phase calculations for all transmission lines were performed by Linecalc in ADS to achieve proper design parameters of signal distribution.

Once the 2-way WPD design was successfully simulated, the subsequent stages were limited to designing 4-way and 8-way WPD layouts, all of which used microstrip lines and the MLIN component (see, Figure-3). These designs' performance reviews were done using Momentum co-simulation, which combines the action of lumped parts and the physical layout to forecast practical performance. After the successful simulation of lower order configurations, the last step was designing of a 16-way divider/combiner as shown in Figure-4.

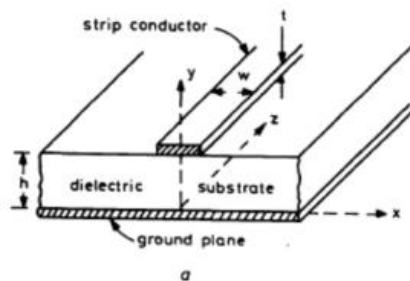


Figure 2. Micro-strip Substrate [23].

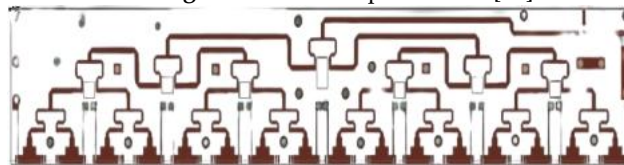


Figure 4. Design layout of Way divider/ combiner

Due to the presence of lumped components (resistors) in the design, co-simulation of Momentum was necessary to quantify the performance of the 16-way divider/combiner accurately. The co-simulation configuration is demonstrated in Figure 5. Using this methodology we gained the following key performance results in the frequency band of (2.7 – 3.0) GHz:

- **Insertion Loss:** Better than -12.50 dB
- **Return Loss:** Better than -14.6 dB
- **Isolation:** Better than -27.16 dB

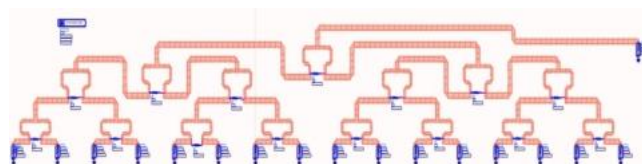
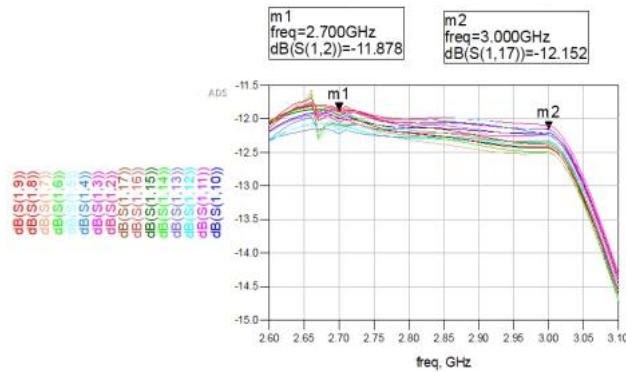


Figure 5. 16-Way Co-Simulation Design

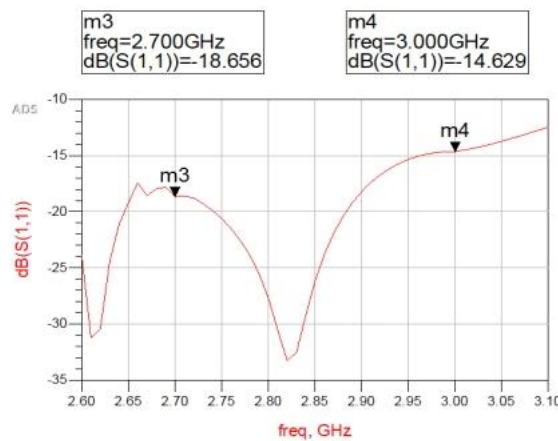
These results satisfied the design criteria, as seen in Figures 6, 7 and 8. Table 2 gives a comparison of performance parameters for the different WPD designs. From the data, it is apparent that the 16-way WPD showed the best overall performance; this shows its suitability for high power applications in the proposed radar system.

**Table 2.** Simulation results summary of 2-way, 4-way, 8-way and 16-way WPD Design

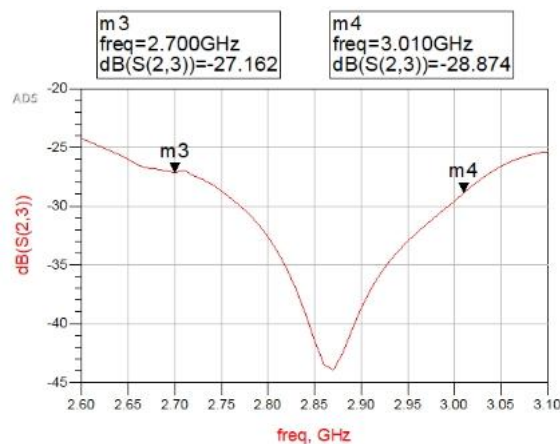
Attributes	2-Way	4-Way	8-Way	16-Way
Insertion Loss	-3 dB	-6.28dB	-9.25dB	-12.181 to -12.5 dB
Return Loss	-20.9 dB	-17.7dB	-11.9dB	-18.65 dB
Isolation	< -18 dB	<-20.45 dB	< -20.45 dB	< -25 dB



**Figure 6.** Insertion loss of Co-simulation of 16-way Wilkinson PCD



**Figure 7.** Return Loss Co-simulation of 16-way Wilkinson PCD



**Figure 8.** Isolation Co-simulation of 16-way Wilkinson PCD

### 3.4. RF Power Amplifier Design

After that successful design of the 16 way Wilkinson Power Divider was completed, then it became necessary to amplify the signal from the pre amplifier to an output power of 1 kW. In order for this to



happen, each of the 16 output ports of WPD was required to generate 75W of power. For this reason PH-2731-75L RF transistor was selected in the fact that it can continuously generate 75W output power under the frequency interval of interest (2.7-3.0 GHz).

Impedance matching was then applied after the choice of the amplifier was made to guarantee optimum power transfer from the RF signal to the input terminal of the transistor. The impedance matching was made precise through the use of the Smith chart utility tool in the ADS software environment which was used in this approach.

The input impedances of the transistor provided in datasheet are enumerated in Table 3. The aim of impedance matching process is to match the input impedance of the RF transistor to the characteristic impedance of incoming RF signal (usually 50 Ω) to optimally transfer the power from the source to the transistors input terminal. Correct impedance matching minimizes your signal loses and does not cause any reflection that is essential for not losing the efficiency of the overall design of the amplifier. Four-micro-strip transmission lines are used whose impedances and angles are tabulated in Table 4.

Table 3. input Impedance

F(GHz)	Z IN (Ω)
2.7	6.9-j12.2
2.9	6.0-j11.7
3.1	5.2-j10.0

Table 4. Impedance and Angle

TLIN#	Impedance, Z(Ω)	Angle (Deg)
TLIN 1	46	57
TLIN 2	25	14
TLIN 3	18.1	17.466
TLIN 4	8.8	18.6

Next step is to implement matching network in hardware. For this purpose, design is implemented in Rogers’s 5870 substrate. The dimensions of micro-strip lines computed using linecalc tool are tabulated in Table 5. The schematic is designed in ADS using MLIN component available in ADS library as shown in Figure 9.

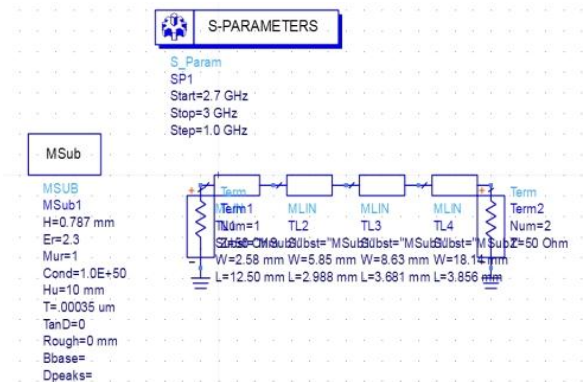


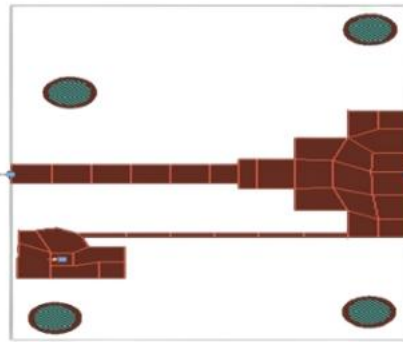
Figure 9. MLIN Component Available in ADS Library

Table 1. Trace Width and Trace Length

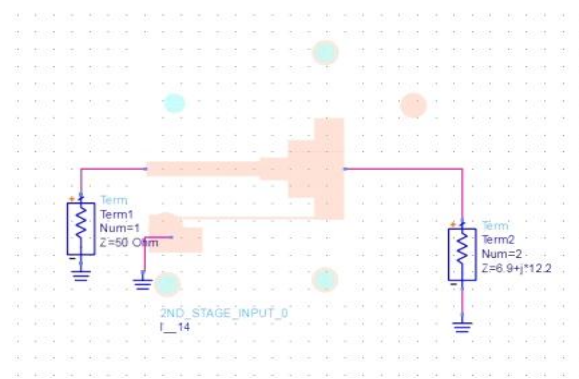
Transmission line sections	Trace Width(mm)	Trace Length(mm)
TLIN 1	2.58	12.50
TLIN 2	5.85	2.988
TLIN 3	8.643	3.681
TLIN 4	18.14	3.856



Afterwards design layout is implemented in ADS using MLIN micro-strip transmission lines available in ADS as shown in Figure 10 and co-simulation layout in Figure 11.

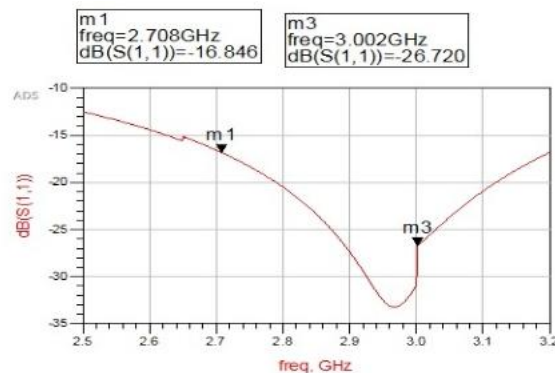


**Figure 10.** Micro-strip Transmission Lines Available In ADS



**Figure 11.** Results of Input Matching Network

In momentum co-simulation results, it was observed that return loss better than  $-16.8\text{dB}$  in 2.7 to 3GHz frequency band is achieved which implies that input matching network is designed successfully. Result of return loss is shown in Figure 12.



**Figure 12.** Return Loss of input matching network

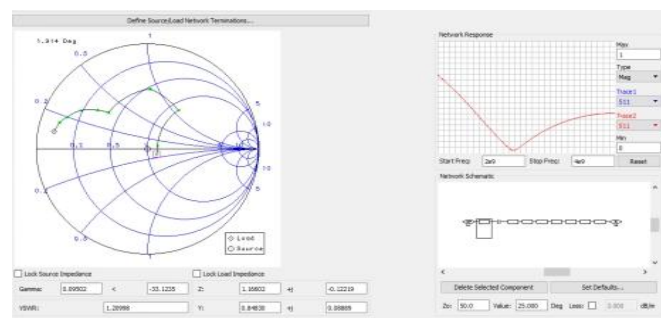
The transistor output impedances available in the data sheet. The goal is to match these impedances to the impedance of RF signal which is  $50\ \Omega$  for maximum power transfer from output terminal of transistor to the load. Transistor output impedance matching is done by using the smith chart utility tool available in ADS. Transistor output impedance matching is done by using smith chart utility tool available in ADS as shown in Figure13. Eight micro strip transmission lines are used whose impedances and angles are tabulated in Table 7. Next step is to implement matching network in hardware. For this purpose, design is implemented in Rogers's 5870 substrate. The dimensions of micro-strip lines computed using line calc tool are tabulated in Table 8. The schematic is designed in ADS using MLIN component available in ADS library as shown in Figure 13.

**Table 7.** Impedance & Angle

	Impedance, $Z(\Omega)$	Angle (Deg)
TLIN 1	46	57
TLIN 2	25	14
TLIN 3	18.1	17.4
TLIN 4	8.8	18.6
TLIN 5	5.1	15
TLIN 6	4.3	16.4
TLIN 7	3.1	17.2
TLIN 8	2.6	13

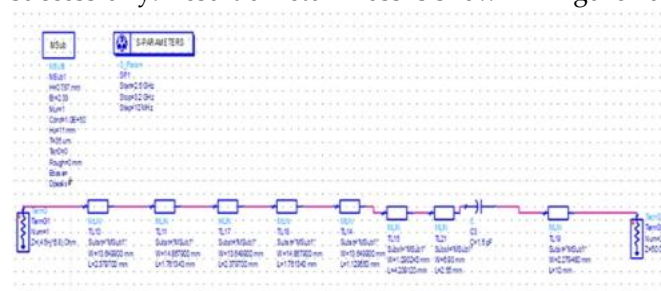
**Table 8.** Trace Width and Trace Length for Eight Transmission lines

Transmission line sections	Trace Width(mm)	Trace Length(mm)
TLIN 1	2.58	12.502
TLIN 2	5.85	2.988
TLIN 3	8.643	3.681
TLIN 4	18.14	3.856
TLIN 5	20.32	3.581
TLIN 6	23	2.856
TLIN 7	26.76	10.507
TLIN 8	29.10	4.988



**Figure 13.** Smith Chart Utility Tool Available in ADS

Design layout is implemented in ADS using MLIN micro-strip transmission lines available in ADS as shown in Figure 14. Next step is to implement momentum Co-simulation to compute the results of input matching network. Design is shown in Figure 15. In momentum co-simulation results, it was observed that return loss better than -8.9dB in 2.7 to 3 GHz frequency band is achieved which implies that output matching network is designed successfully. Result of return loss is shown in Figure 16.



**Figure 14.** Final Power Amplifier Schematics Design

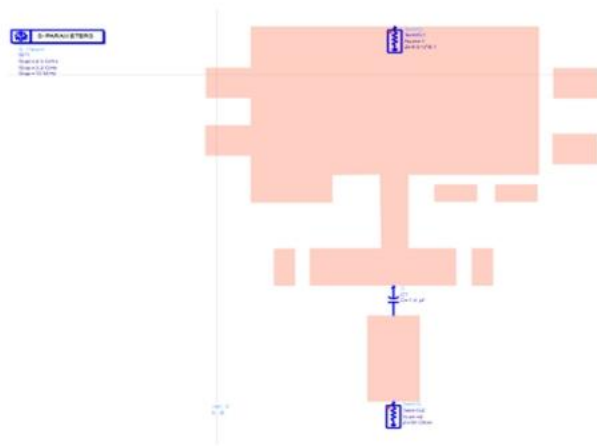


Figure 15. Design layout of FPA

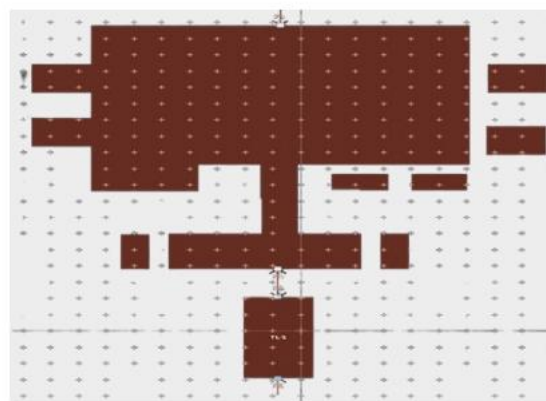


Figure 16. Input Matching Network Layout Design

#### 4. Results and Discussion

The measurement is divided into two main parts; results of 16-way divider/ combiner measured using vector network analyser part number E5071C. After that testing of complete amplifier design along with 16-way divider / combiner was implemented. To evaluate performance of 16-way Divider / Combiner prototype is physically tested with Agilent vector network analyser (part number E5071C). S parameters are recorded to validate the performance. Input from VNA is fed to port 1 while the output is taken from port 2 to port 17. Since VNA is a two-port device, therefore 15 remaining ports were terminated with 50Ω load [23]. The test setup diagram is shown in Figure 17. Scattering parameters are measured to estimate Insertion loss. Insertion loss measured at port 2 is displayed in Figure 18. The data collected from port2 to port17 is tabulated in Table 9.

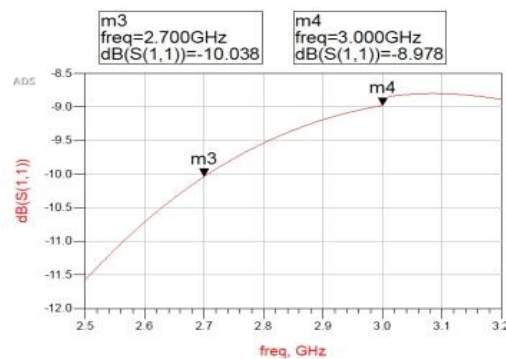
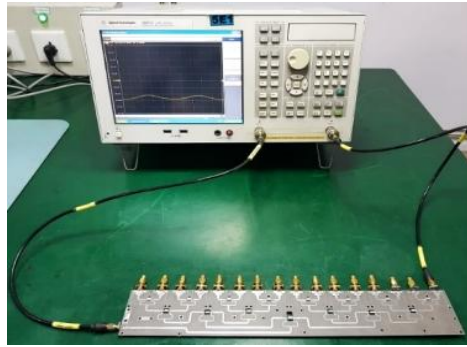


Figure 17. Result of Return Loss



**Figure 18.** Testing of 16.1 Power Divider/ Combiner with Vector Network Analyzer.

**Table 9.** Insertion Loss in dB

Insertion Loss (dB)	2.7GHz	2.8GHz	2.9 GHz	3.0 GHz
S <sub>21</sub>	-12.553	-12.596	-12.633	-12.685
S <sub>31</sub>	-12.412	-12.466	-12.621	-12.688
S <sub>41</sub>	-12.544	-12.506	-12.590	-12.576
S <sub>51</sub>	-12.325	-12.588	-12.644	-12.544
S <sub>61</sub>	-12.466	-12.612	-12.690	-12.566
S <sub>71</sub>	-12.621	-12.624	-12.498	-12.671
S <sub>81</sub>	-12.783	-12.429	-12.689	-12.689
S <sub>91</sub>	-12.590	-12.661	-12.577	-12.694
S <sub>101</sub>	-12.541	-12.577	-12.611	-12.734
S <sub>111</sub>	-12.447	-12.499	-12.476	-12.722
S <sub>121</sub>	-12.544	-12.510	-12.492	-12.667
S <sub>131</sub>	-12.559	-12.568	-12.621	-12.632
S <sub>141</sub>	-12.355	-12.598	-12.587	-12.651
S <sub>151</sub>	-12.422	-12.499	-12.729	-12.597
S <sub>161</sub>	-12.509	-12.523	-12.677	-12.584
S <sub>171</sub>	-12.412	-12.589	-12.680	-12.624

#### 4.1. Comparison of Simulated and Measured Results

The data collected from measurements and simulations is plotted on the graph in MATLAB as shown in Figure 19 and Table 10. The comparison shows that designed WPD perfectly aligns with the simulated results over the designated frequency range (see, Figure 20).

**Table 10.** Comparison between Simulated and actual results

Insertion Loss (dB)	Simulated Results at 2.7 GHz	Measured Results at 2.7 GHz	Simulated Results at 3.0 GHz	Measured Results at 3.0 GHz
Port 2	-11.872	-12.553	-12.143	-12.685
Port 3	-12.112	-12.412	-12.353	-12.688
Port 4	-12.324	-12.544	-12.656	-12.576
Port 5	-12.184	-12.325	-12.487	-12.544
Port 6	-11.982	-12.466	-12.543	-12.566

Port 6	-12.429	-12.621	-12.633	-12.671
Port 7	-12.564	-12.783	-12.766	-12.689
Port 8	-12.185	-12.590	-12.872	-12.694
Port 9	-11.655	-12.541	-12.674	-12.734
Port 10	-12.336	-12.447	-12.432	-12.722
Port 11	-12.324	-12.544	-12.766	-12.667
Port 12	-12.244	-12.559	-12.566	-12.632
Port 13	-11.776	-12.355	-12.764	-12.651
Port 14	-12.673	-12.422	-12.893	-12.597
Port 15	-12.877	-12.509	-12.236	-12.584
Port 16	-12.335	-12.412	-12.187	-12.624

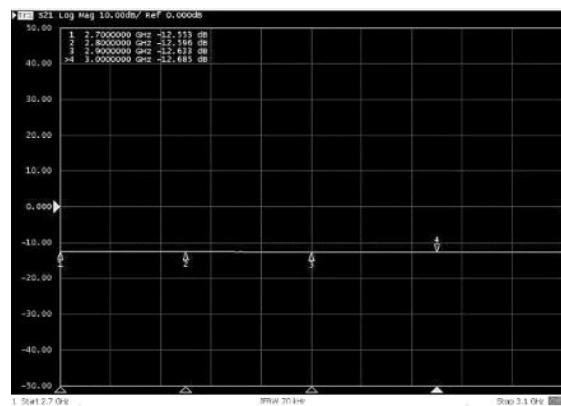


Figure 19. Measured Results of 16.1 Power Divider / Combiner

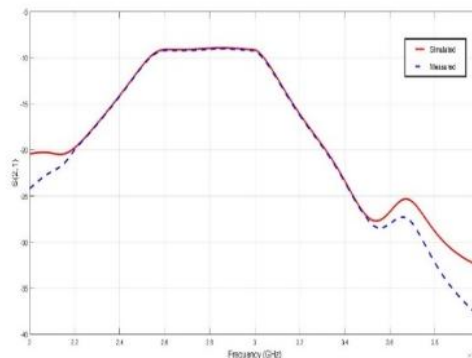


Figure 20. Measurement Vs Simulation Results

#### 4.2. Test setup for Amplifier Testing

An Agilent E4428C RF signal generator, modulated with 10% duty cycle pulses at +30 dBm, was used to stimulate the amplifier within the 2.7-3.0 GHz band. The signal was amplified to approximately 54 dBm through a low-loss cable and pre-amplifier before driving the power amplifier. A 50-dB attenuator (DTS-500) was employed to protect the Agilent E4440A spectrum analyzer from the high-power output exceeding +30 dBm. Characterization of the 16-way divider/combiner using a vector network analyzer revealed a minor 0.5 dB deviation in insertion loss compared to simulations, attributed to connector and cable losses. Subsequent testing confirmed the RF amplifier's output power to exceed 1 kW within the operational band, validating the effectiveness of the designed matching networks.

The results of the designed and fabricated device under test in test setup as shown in Figure 21 depict that average amplification of 60 dBm within the frequency band of 2.7GHz to 3.0 GHz is achieved as per

requirements. The graphical depiction from RF signal generator to spectrum analyzer is shown in Figure 22. The output powers viz-a-viz transmitted frequencies are shown in the Table 11.

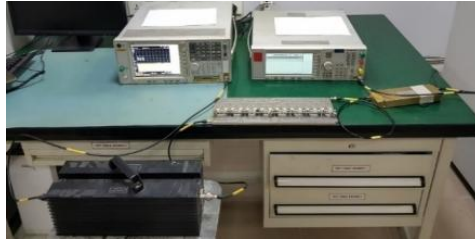


Figure 21. Test Setup. Block Diagram

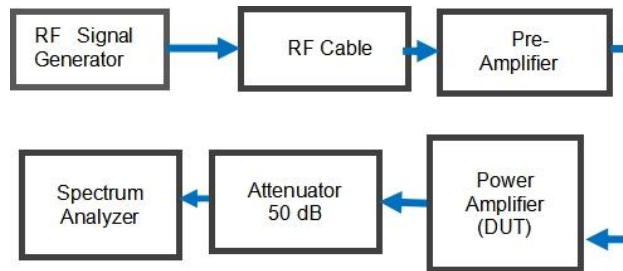


Figure 22. DUT Test Setup

Table 11. Final DUT Results

Frequency	Output Power
2.7 GHz	60.84 dBm
2.8 GHz	60.26 dBm
2.9 GHz	61.24 dBm
3.0 GHz	59.97 dBm

## 5. Conclusion

This work reports design, simulation, fabrication and experimentation results of a high efficiency 1:16 Wilkinson Power Divider/Combiner (PD/Combiner) coupled with amplifier impedance matching. The study examined behaviour & characteristics of the PD/combiner during the design process. The design methodology was performed on two stages in the Advanced Design System (ADS) 2016 software using Rogers RT/Duroid 5870 as the substrate material. Further re-simulations of course showed good results, with an insertion loss of -12.5 dB, a return loss of -18.565 dB and an isolation of -25 dB for the PD/combiner.

Following from the successful simulation results, a layout of a printed circuit board (PCB) was created and fabricated. After fabrication the module was tested using an Agilent vector network analyzer (E5071C). Measured results confirmed great performance, with -25.5 dB isolation and -12.14 dB insertion loss. Also, the amplifier design was successfully designed to fit the fabricated PD/combiner and resulted in a 1 kW output power within the specified custom size constrains. The output power was checked using an Agilent Spectrum Analyzer (E4440A), after the procedures from the results section.

Our work also identifies that although dramatic improvements have been achieved in the PD/combiner and the amplifier systems design of radar RF power transmitters and transmitter system design, room for further improvement still exists, especially for custom systems. As the technology of radar is further developed, there is an eternal need for the miniaturized, budget-friendly options. Future work could be concerned with minimizing insertion loss for the PD/combiner even more. Other simulations were also performed in addition to the 1:16 Wilkinson Power Divider fabrication including 2-way, 4-way and 8-way WPDs which may be of value in future research ventures.

**Funding:** This research received no external funding.

**Acknowledgments:** In this section, you can acknowledge any support given which is not covered by the author contribution or funding sections. This may include administrative and technical support, or donations in kind (e.g., materials used for experiments).

**Conflicts of Interest:** The authors declare no conflict of interest.



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